Amendments to the Specification:

Please replace paragraph 1, beginning on line 3.

The present application is related to the following listed seven applications: "Serial No. ———— 10/016,772 (RPS920010126US), entitled "Method and System for Use of an Embedded Field Programmable Gate Array Interconnect for Flexible I/O Connectivity;" "Serial No. ———— 10/016,449 (RPS920010127US1), entitled "Method and Use of a Field Programmable Gate Array (FPGA) Function Within an Application Specific Integrated Circuit (ASIC) to Enable Creation of a Debugger Client Within the ASIC;" Serial No. ———— 10/016,448 (RPS 920010128US1), entitled "Method and System for Use of a Field Programmable Function Within an Application Specific Integrated Circuit (ASIC) To Access Internal Signals for External Observation and Control;" Serial No. ———— 10/015,922 (RPS920010129US1), entitled "Method and System for Use of a Field Programmable Interconnect Within an ASIC for Configuring the ASIC;" Serial No. ———— 10/015,920 (RPS920010130US1), entitled "Method and System for Use of a Field Programmable Function Within a Chip to Enable Configurable I/O Signal Timing Characteristics;" Serial No. ———— 10/015,923 (RPS920010131US1), entitled "Method and System for Use of a Field Programmable Function Within a Standard Cell Chip for Repair of Logic Circuits;" and Serial No. ———— 10/015,921 (RPS920010132US1), entitled "Method and System for Use of a Field Programmable Gate Array (FPGA) Cell for Controlling Access to On-Chip Functions of a System on a Chip (S)C) Integrated Circuit;" assigned to the assignee of the present application, and filed on the same date.